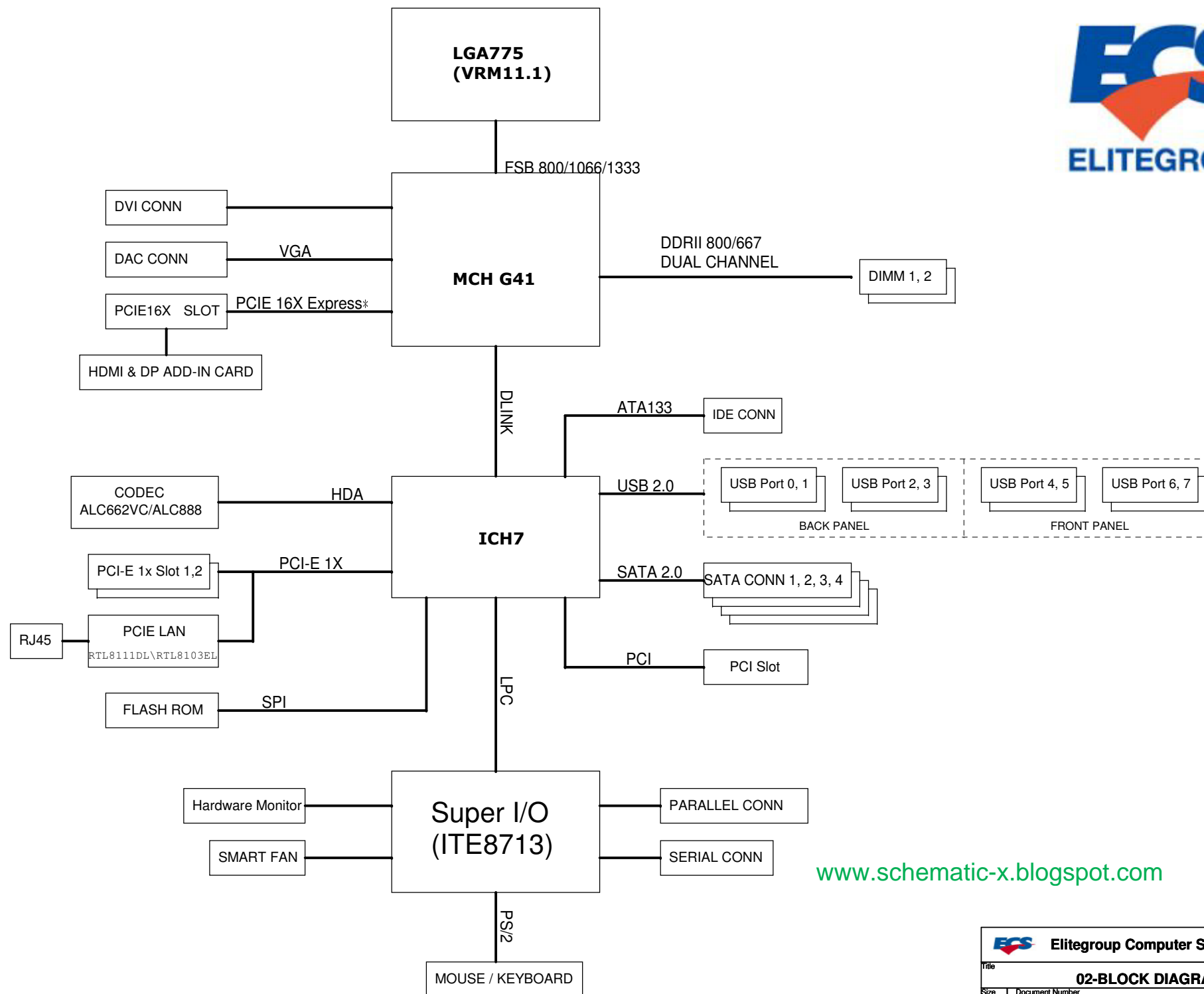


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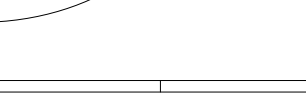
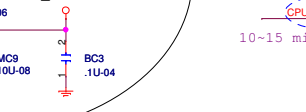
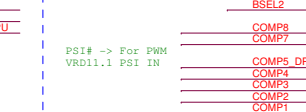
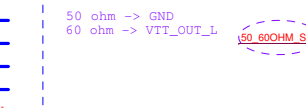
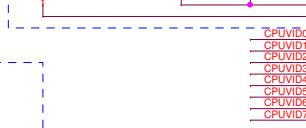
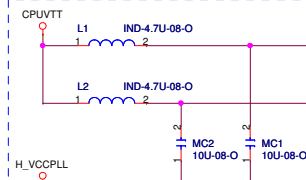


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0 3	-	C P U - H O S T & S I G N A L	
0 4	-	C P U - P W R & G N D	
0 5	-	M C H - H O S T	
0 6	-	M C H - D M I / P C I E / D A C / H D M I	
0 7	-	M C H - M E M O R Y	
0 8	-	M C H - P W R / G N D	
0 9	-	I C H 7 - D M I / P C I E / S A T A / U S B / M I S C 1	
1 0	-	I C H 7 - H D A / R G M I I / S P I / P C I / R T C / M I S C 2	
1 1	-	I C H 7 - P W R / G N D	
1 2	-	C L K G E N I C S 9 L P R S 5 2 5	
1 3	-	D D R 2 D I M M 1 , 2	
1 4	-	D D R 2 T E R M I N A T I O N	
1 5	-	P C I E 1 6 x / 1 x S l o t	
1 6	-	P C I S l o t	
1 7	-	V G A ( R G B )	
1 8	-	U S B	
1 9	-	P C I E L A N ( R T L 8 1 1 1 D L & 8 1 0 2 E L )	
2 0	-	A u d i o C o d e r c ( R e a l t e k A L C 6 6 2 V C / 8 8 8 )	
2 1	-	A u d i o I n t e r f a c e ( 3 P o r t H D A )	
2 2	-	D V I I n t e r f a c e	
2 3	-	S u p e r I / O ( I T E 8 7 1 3 )	
2 4	-	K B / M S / H O L E	
2 5	-	C O M / L P T / R i n g / 1 0 4 L e v e l B O M	
2 6	-	H M / F a n	
2 7	-	V o l t a g e R e g u l a t o r	
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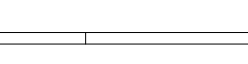
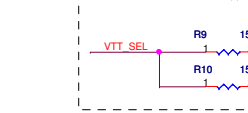
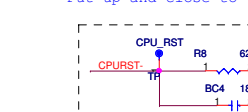
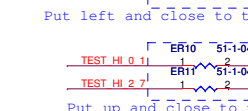
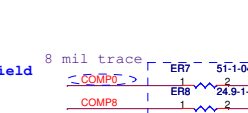
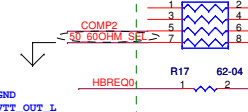
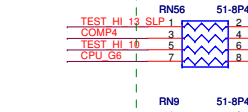
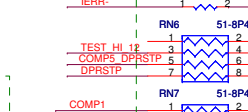
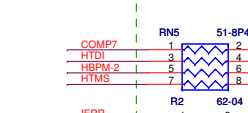
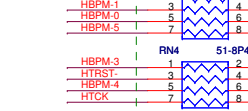
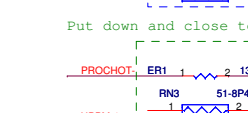
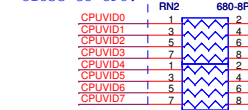


[www.schematic-x.blogspot.com](http://www.schematic-x.blogspot.com)

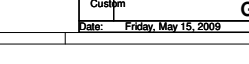
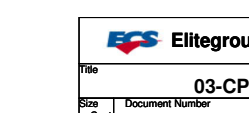
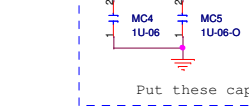
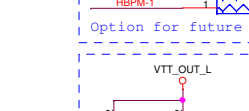
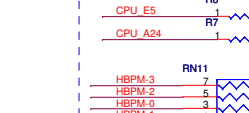
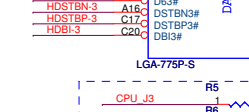
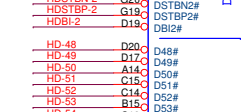
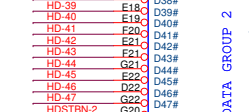
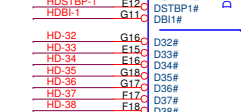
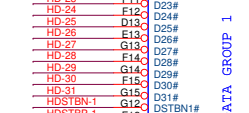
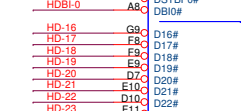
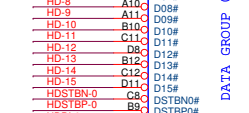
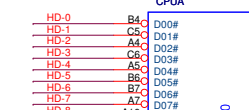
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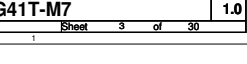
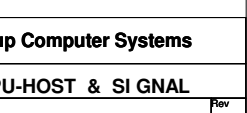
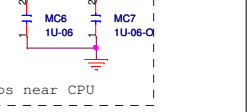
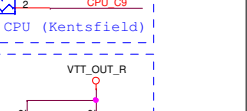
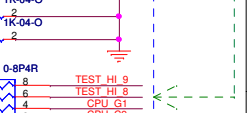
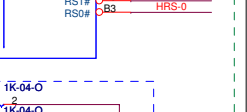
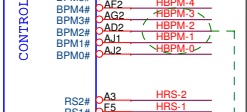
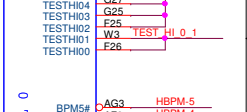
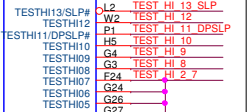
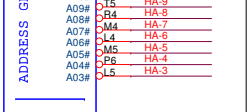
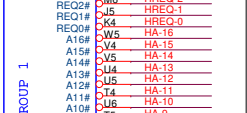
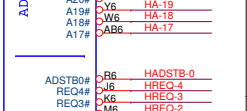
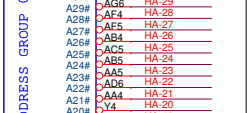
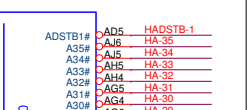
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Close to CPU.

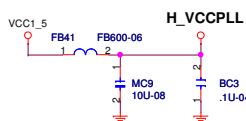


Close to CPU.



Please Close CPU

(1.5V)



根據 Chipset 需求而定  
GTL\_SEL1:2=11 -> 0.667VTT  
GTL\_SEL1:2=10 -> 0.650VTT  
GTL\_SEL1:2=01 -> 0.630VTT  
GTL\_SEL1:2=00 -> 0.615VTT

GTL Level Choice  
By Chipset

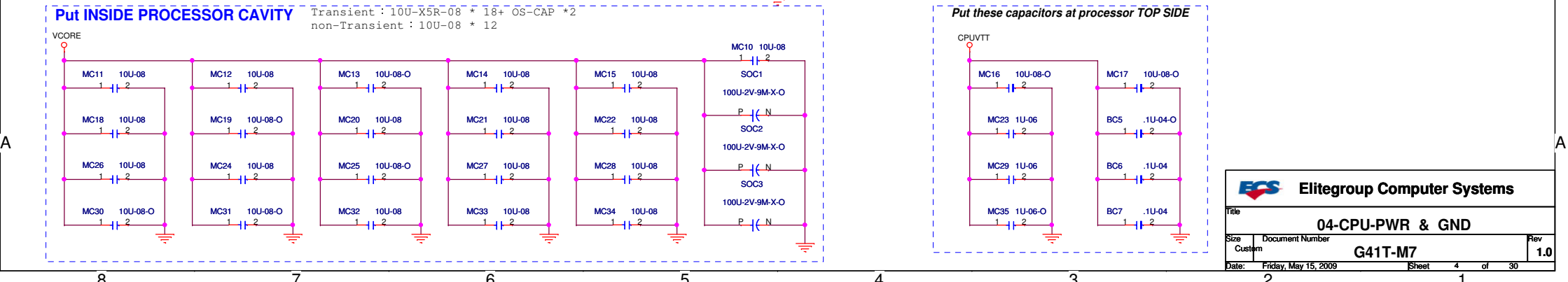
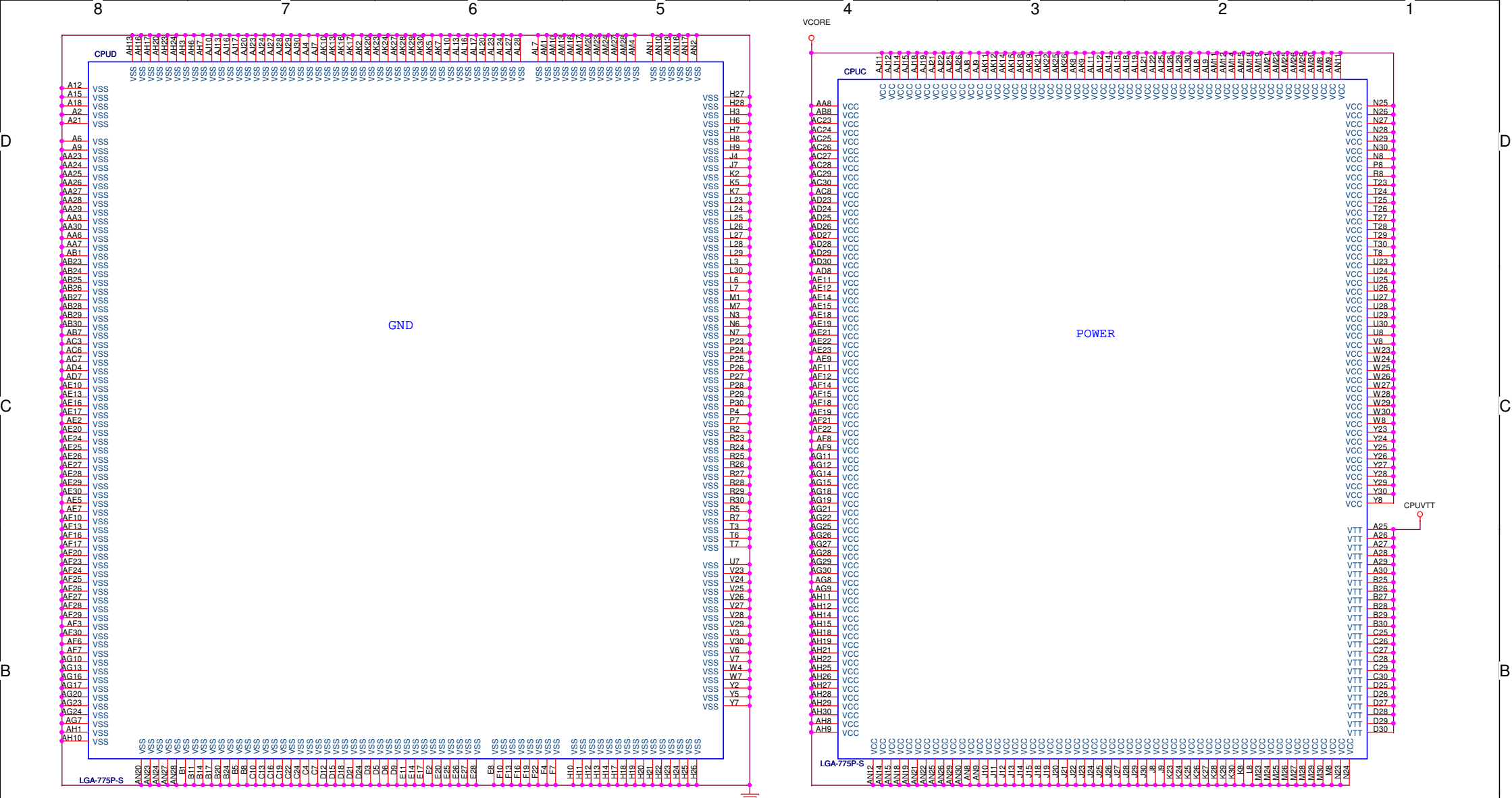
Near CPU no more than 1.5"

Elitegroup Computer Systems

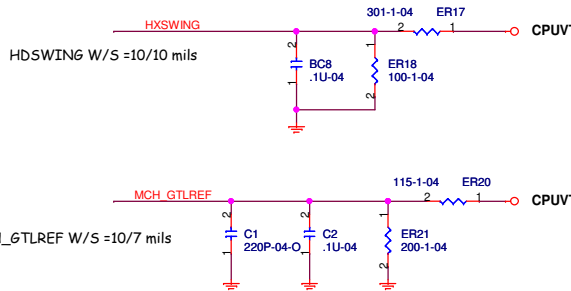
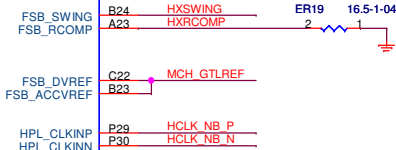
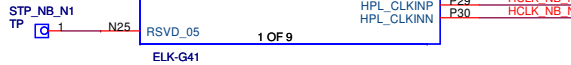
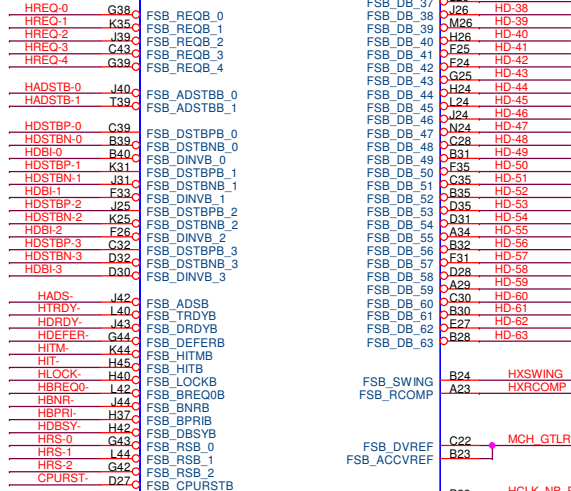
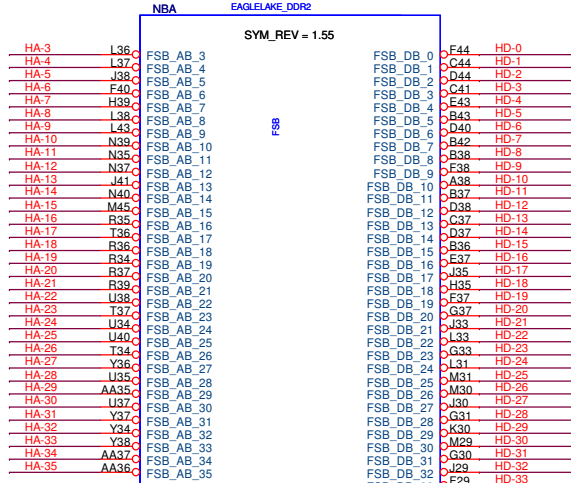
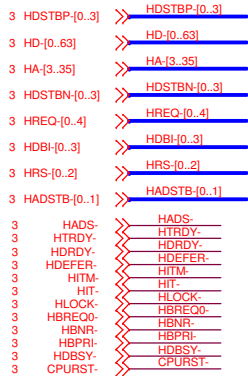
03-CPU-HOST & SI GNAL

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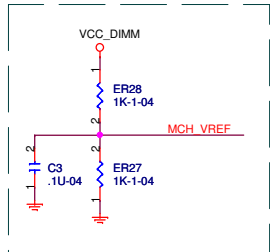
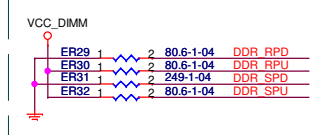
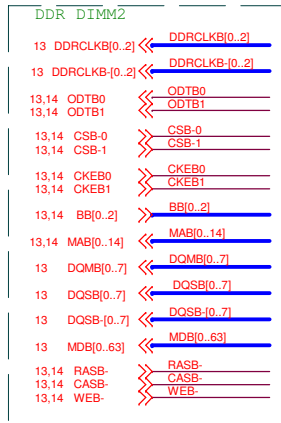
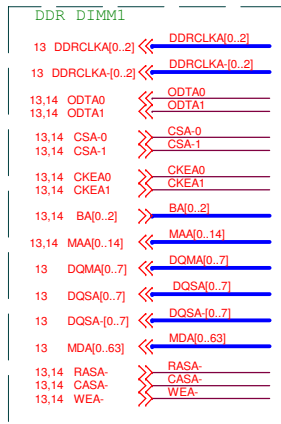
Friday, May 15, 2009



HOST

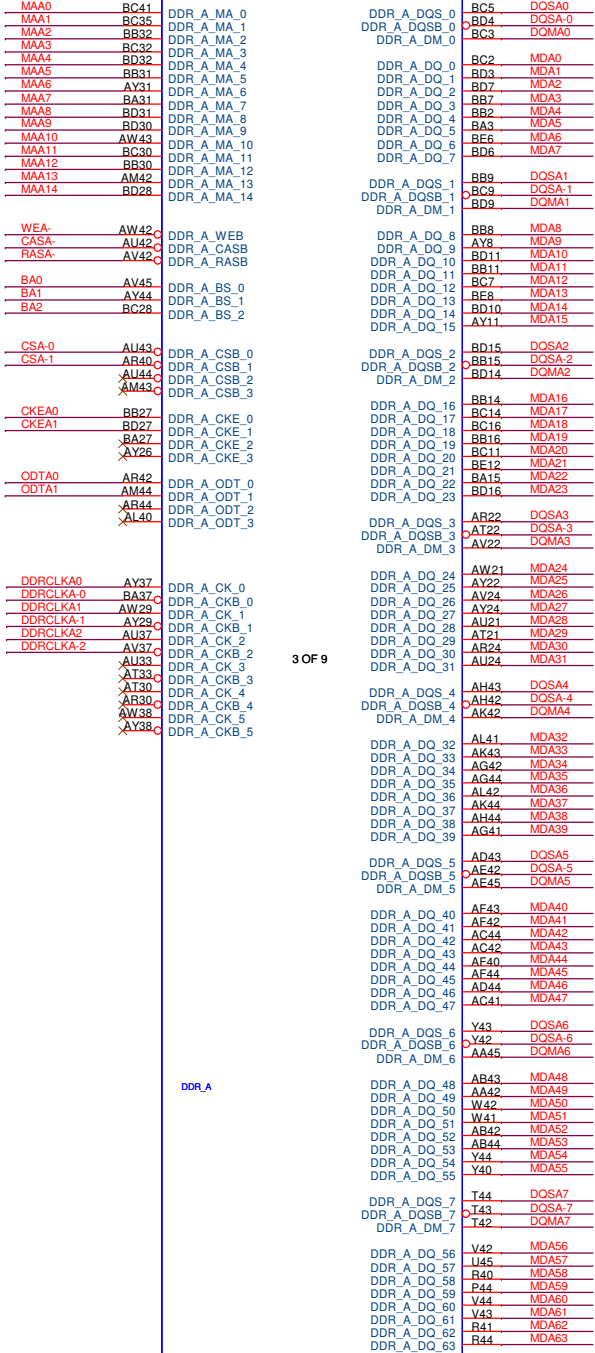






NBC EAGLELAKE\_DDR2

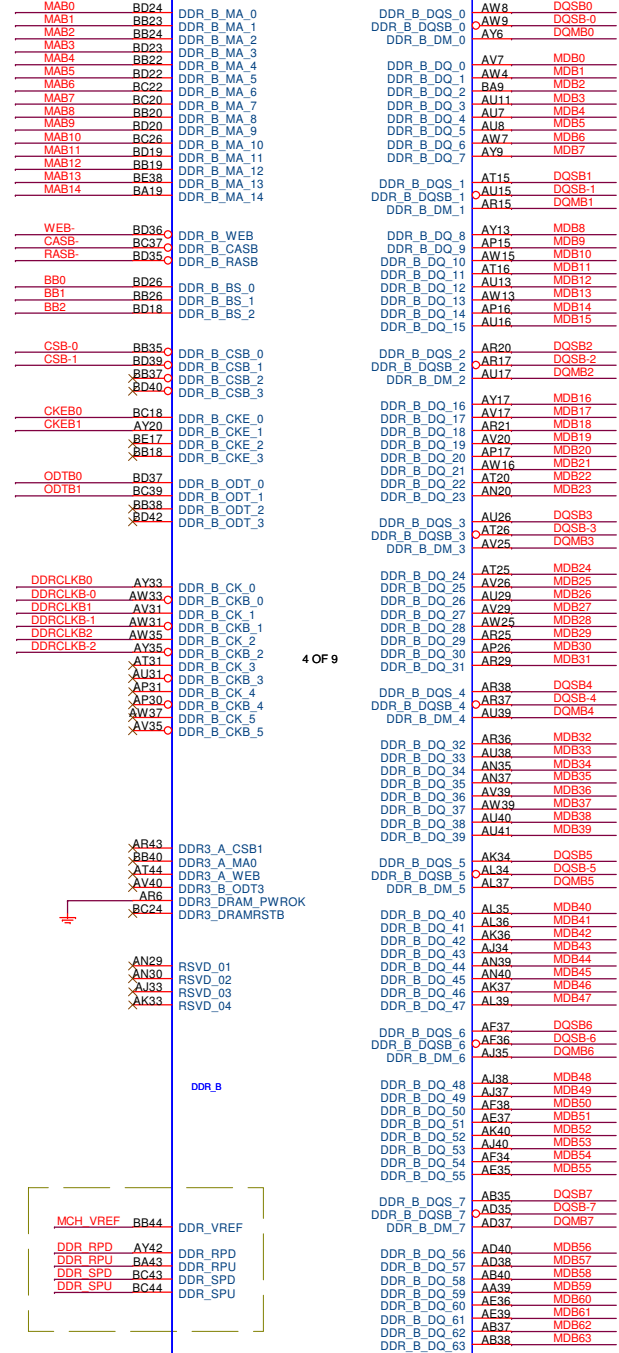
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NBD EAGLELAKE\_DDR2

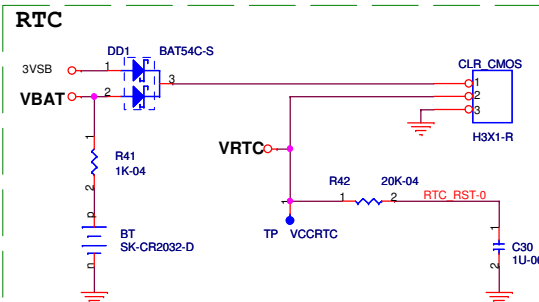
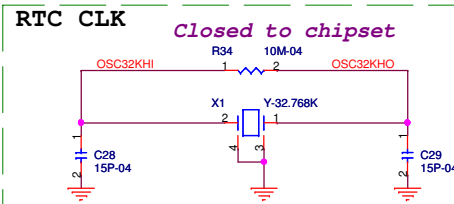
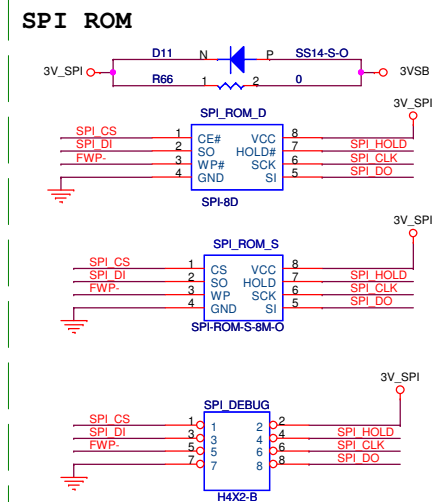
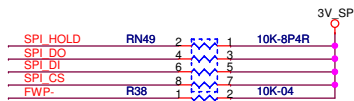
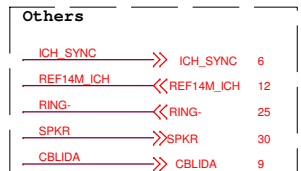
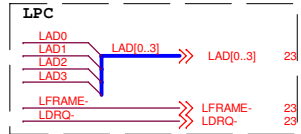
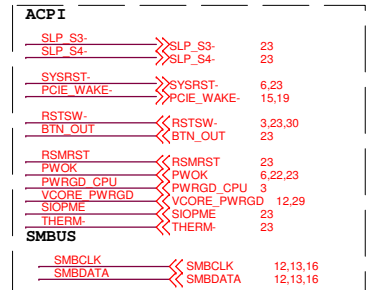
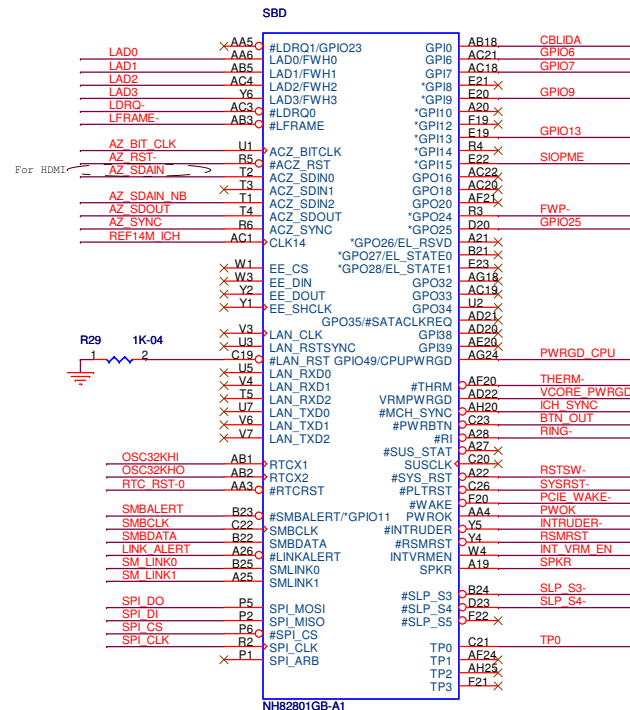
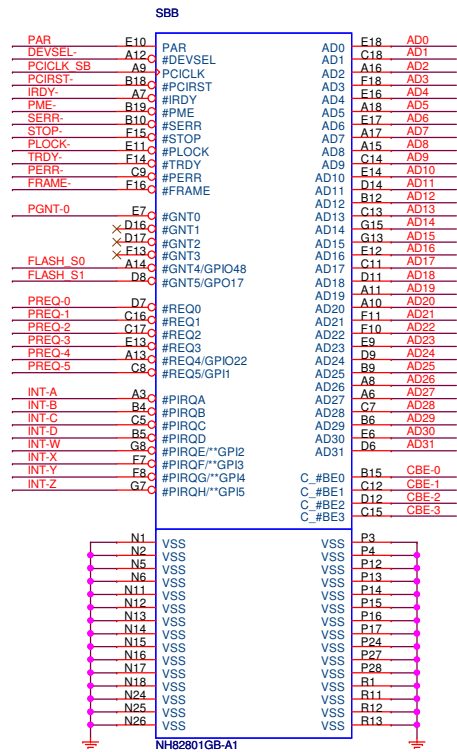
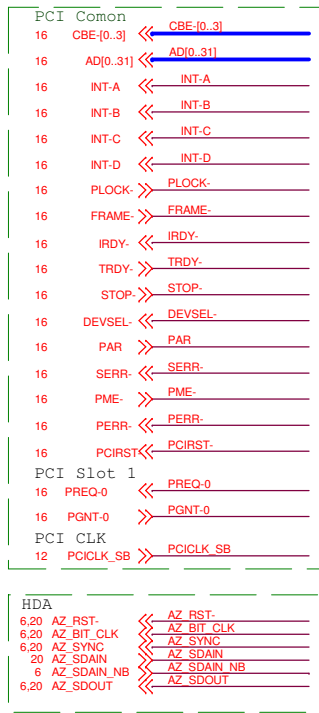
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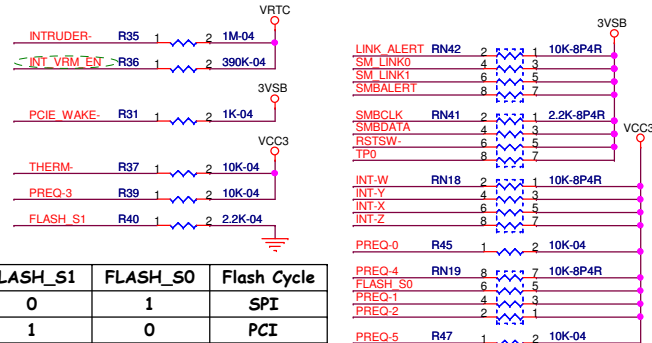
ELK-G41







Strap to Enable  
Internal SUS VRM



FLASH_S1	FLASH_S0	Flash Cycle
0	1	SPI
1	0	PCI
1	1	LPC

	H	Floating	DESCRIPTION
AZ_SDOUT	PCIE 4x *1	PCIE 1x *4	PCIE 1x/4x Select
AZ_SYNC	PCIE 4x *1	PCIE 1x *4	PCIE 1x/4x Select

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Title: 10-I CH7\_HDA/ SPI / PCI / RTC/ MI SC

Size: Custom

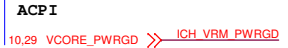
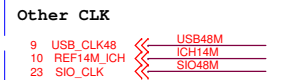
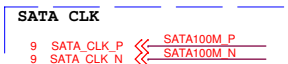
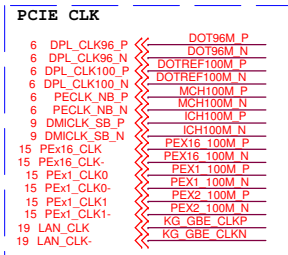
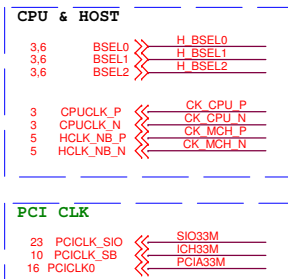
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Date: Friday, May 15, 2009

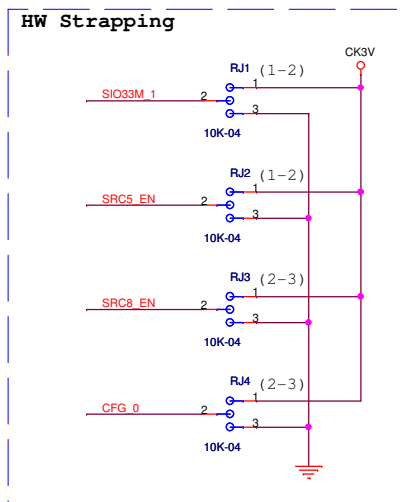
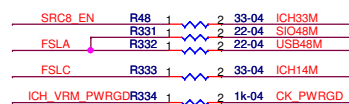
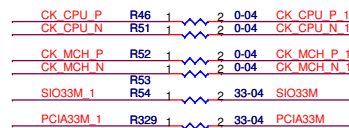
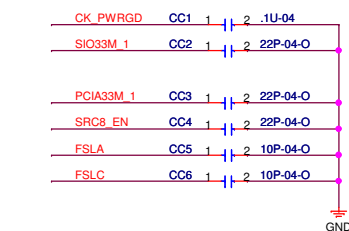
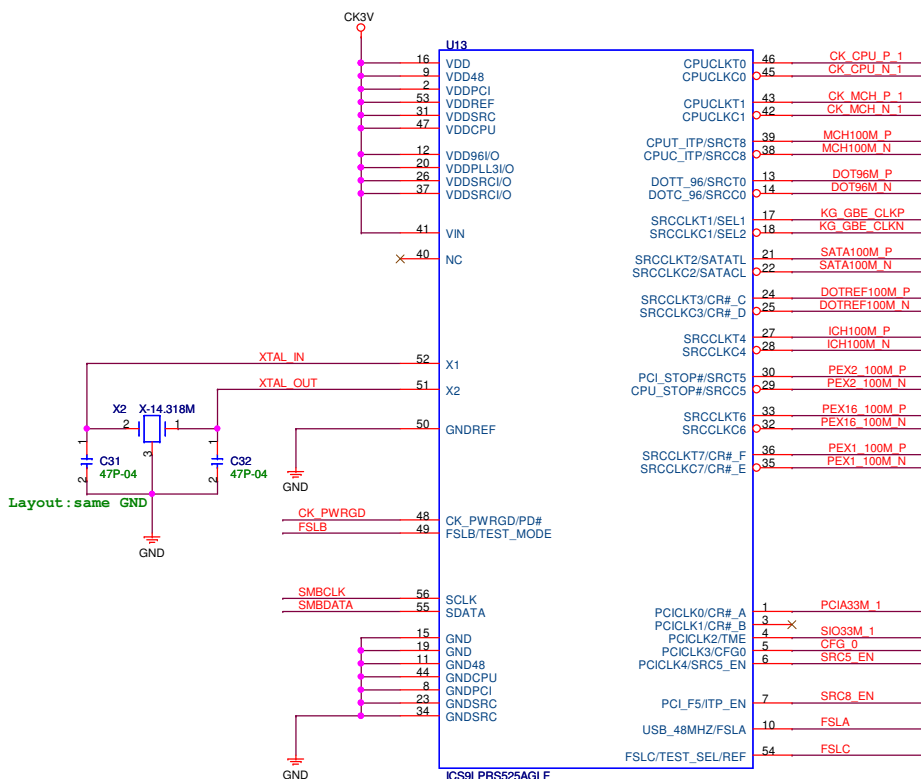
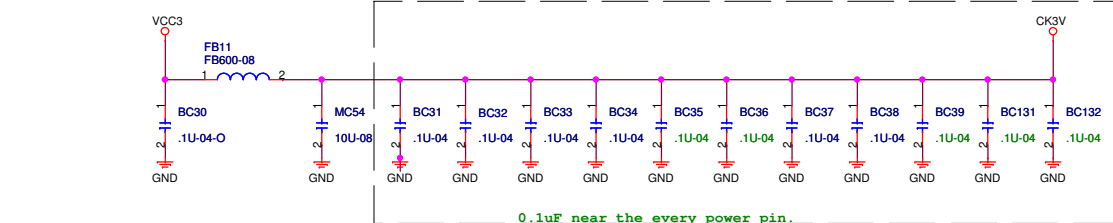
Sheet: 10 of 30

Rev: 1.0





Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU CLOCK (MHZ)	CPU FSB CLOCK
0	0	0	266.66	FSB 1066
0	1	0	200.00	FSB 800
1	0	0	333.33	FSB 1333



FOR ICS9LPRS525AGLF  
PIN 4(TIME)STRAP

PIN 4 (TIME)	
HI	Overclocking of CPU and SRC NOT allowed
LO	Overclocking of CPU and SRC allowed

FOR ICS9LPRS525AGLF  
PIN 5(CFG0)STRAP

PIN 5 (CFG0)	PIN 4 (TIME)	PCI3/CFG0 PLL Mode
LO	X	0
MID	X	1
HI	TME=0	2
HI	TME=1	3

Don't select PLL mode 3,  
it's will effect LAN frequency

FOR ICS9LPRS525AGLF  
PIN 6(SRC5\_EN)STRAP

PIN 6 (SRC5_EN)	PIN 29,30
HI	SRC FUNCTION
LO	CPU & PCI STOP #

FOR ICS9LPRS525AGLF  
PIN 7(ITP\_EN)STRAP

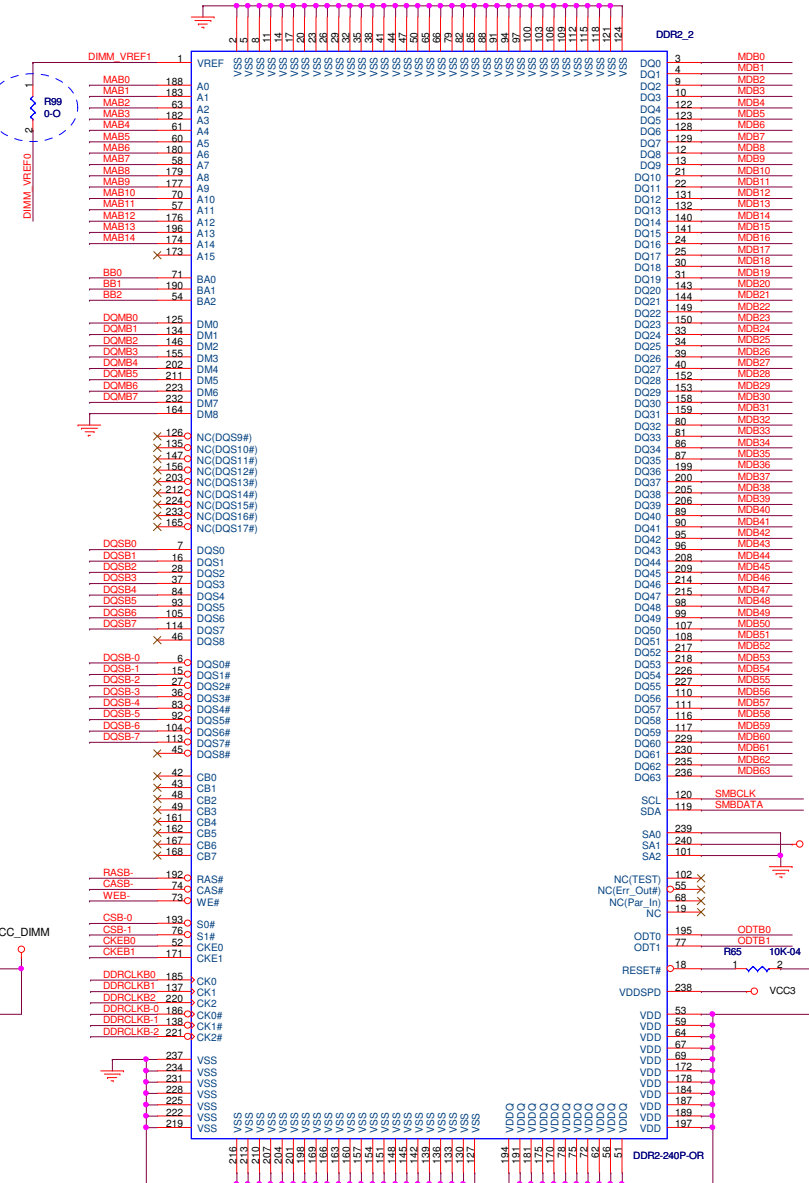
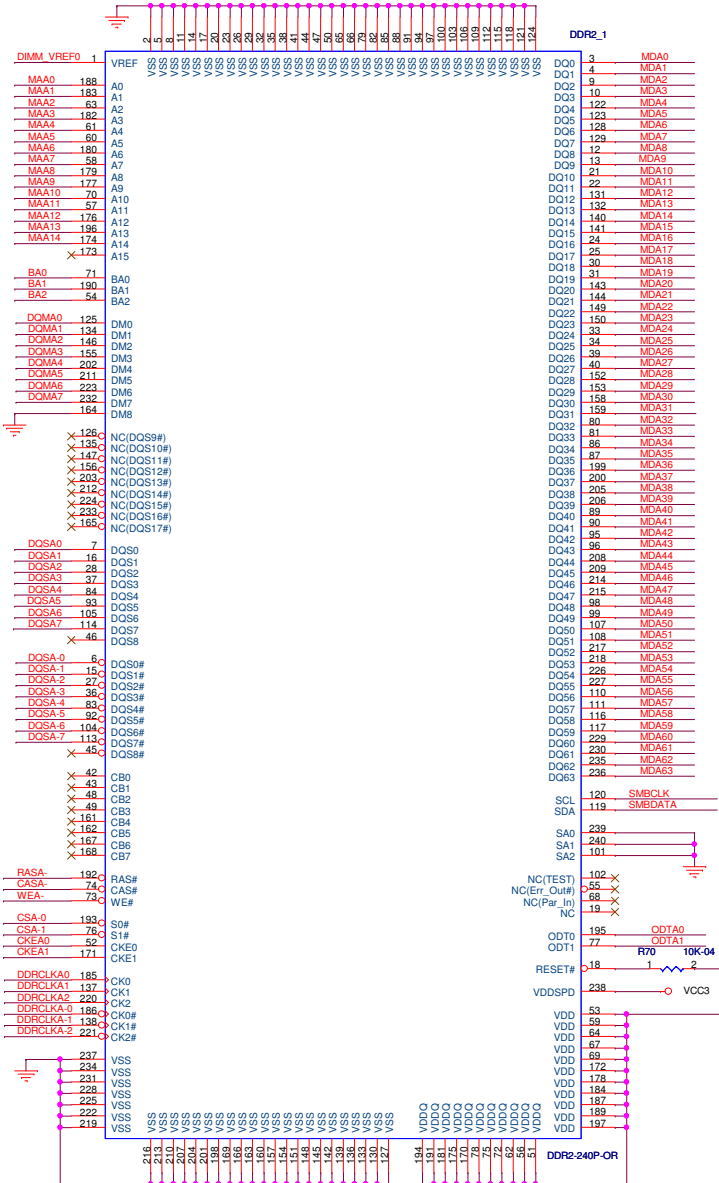
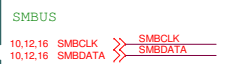
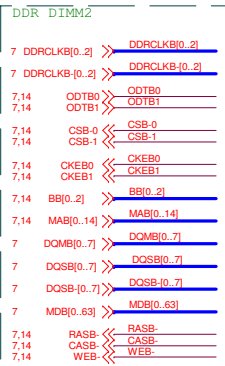
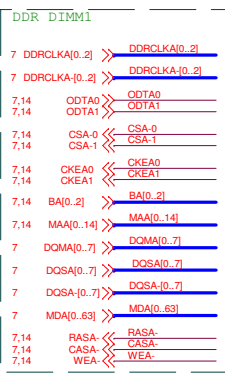
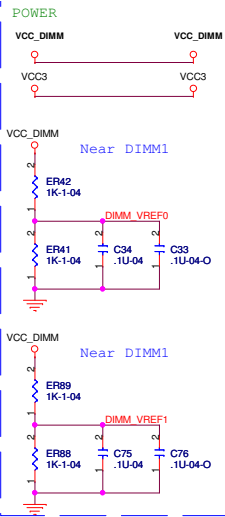
PIN 7 (ITP_EN)	PIN 38,39 MODE
HI	CPU ITP FUNCTION
LO	SRC8

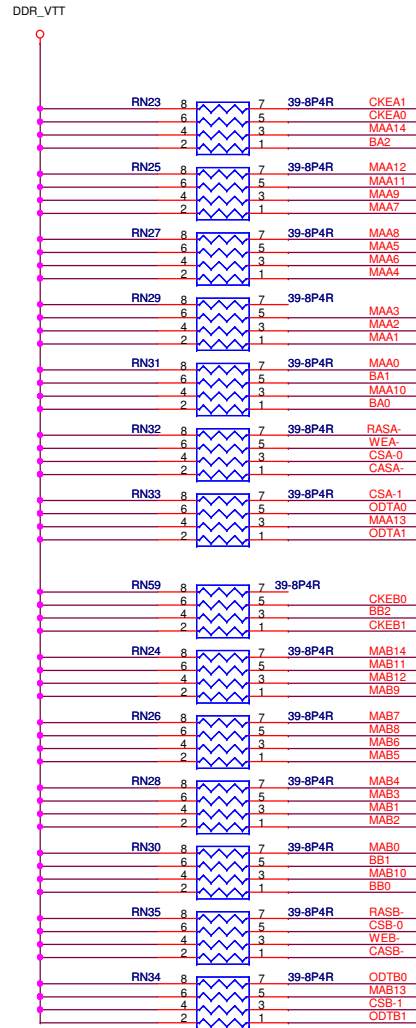
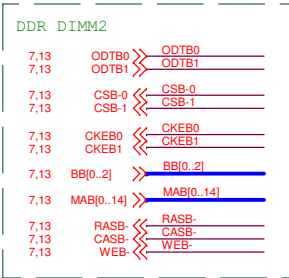
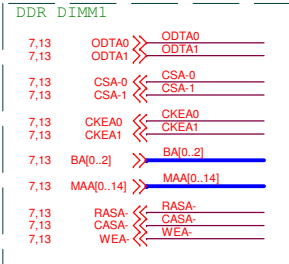
**Elitegroup Computer Systems**

File: **12-I CS9LPRS525**

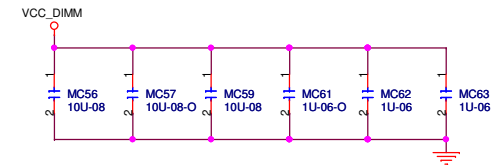
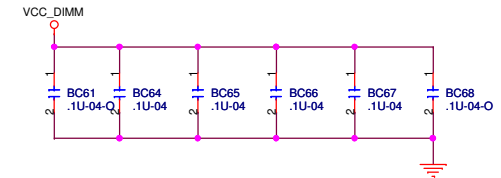
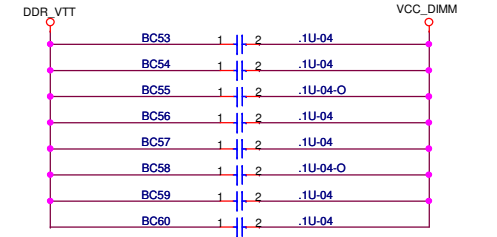
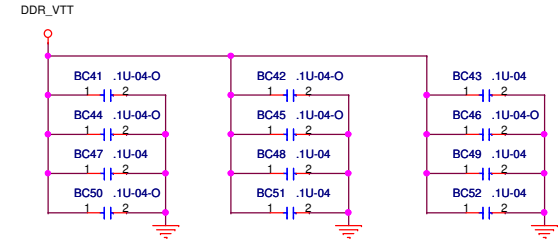
Size: Custom Document Number: **G41T-M7** Rev: **1.0**

Date: Friday, May 15, 2009 Sheet 12 of 30

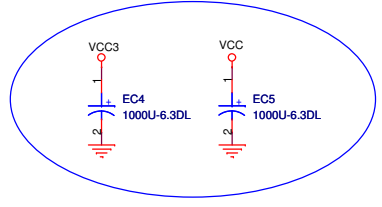
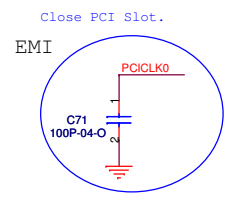
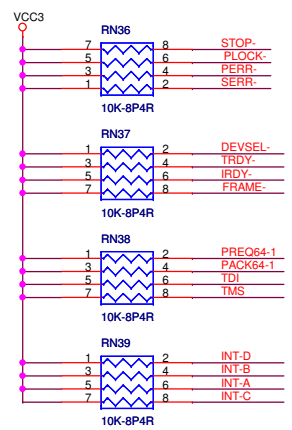
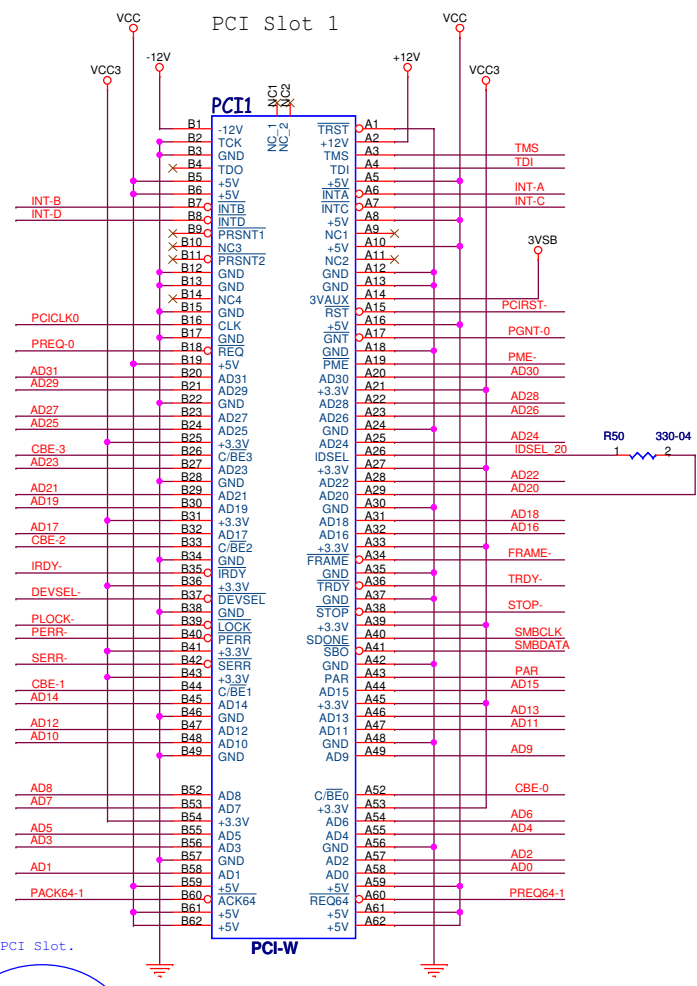
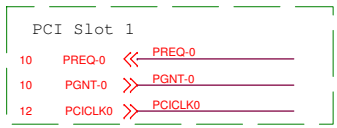
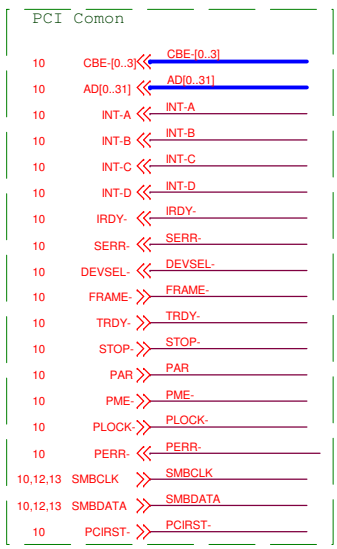




**DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND**  
Placed within 200mils of VTT Termination R-packs

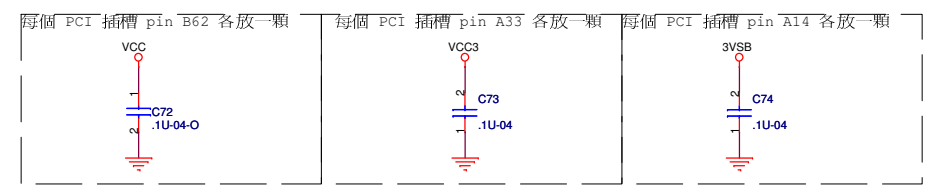


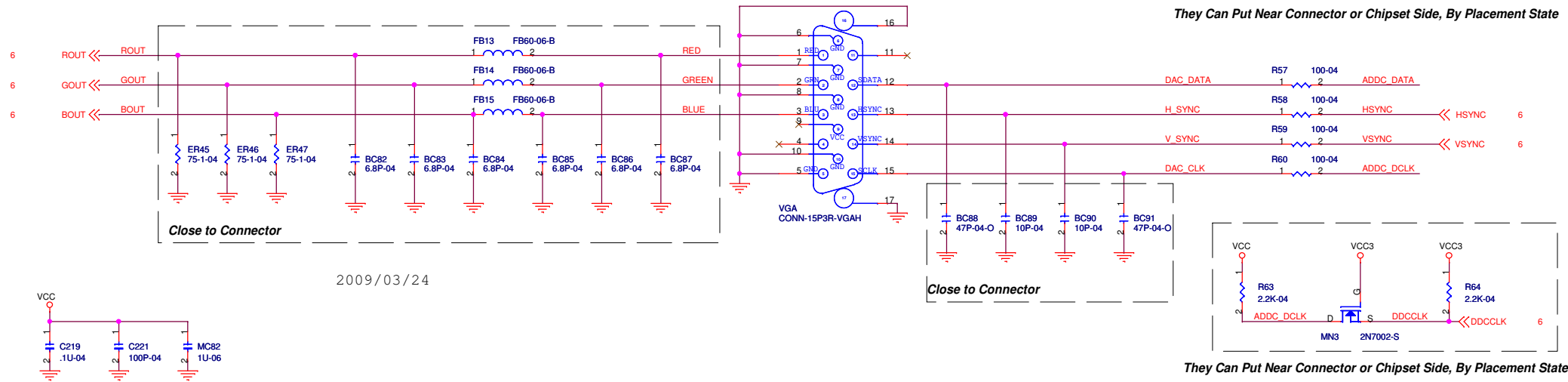


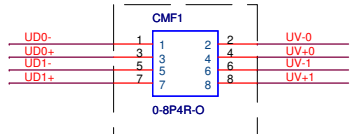
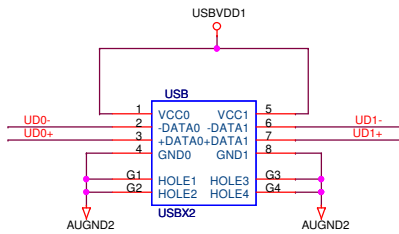
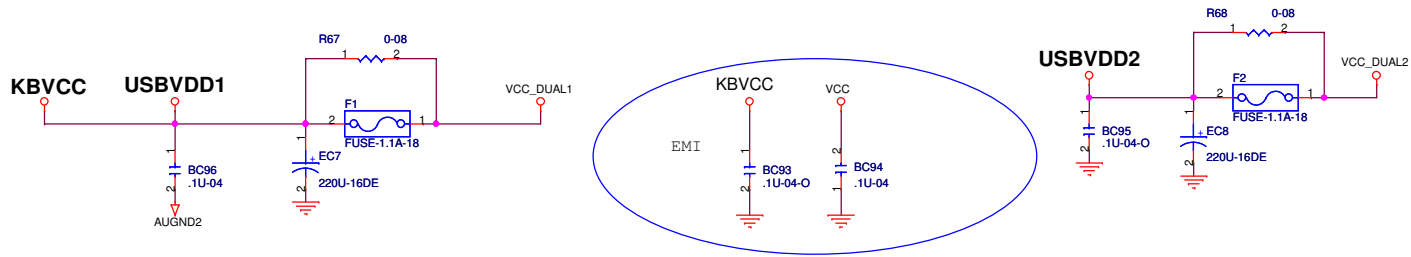
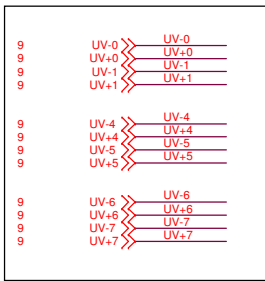


IDSEL=AD20  
INT [A, B, C, D]

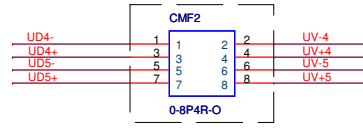
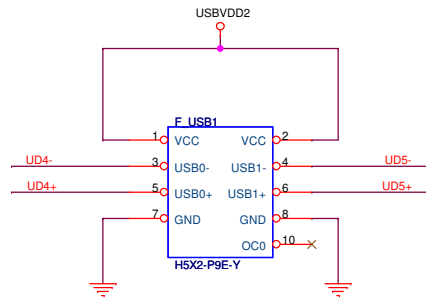
Please place close to PCI1 and PCI2 Slot.



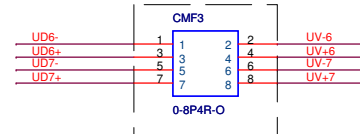
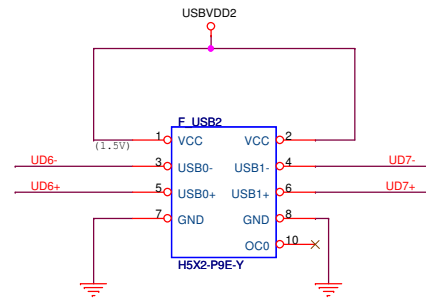




Close to USB connector



Close to header(F\_USB1)



Close to header(F\_USB2)

Pin configuration diagram for the USB VDDIO pin. The diagram shows connections for USBVDDIO, 3VSBD, VCC3, AUGND2, LAN HSIP, LAN HSN, OK PE LANP, OK PE LANN, LAN HSOP, LAN HSON, PCIE WAKE UP, PCIE LAN RST, UV-2, UV+2, UV-3, and UV+3. The connections are as follows:

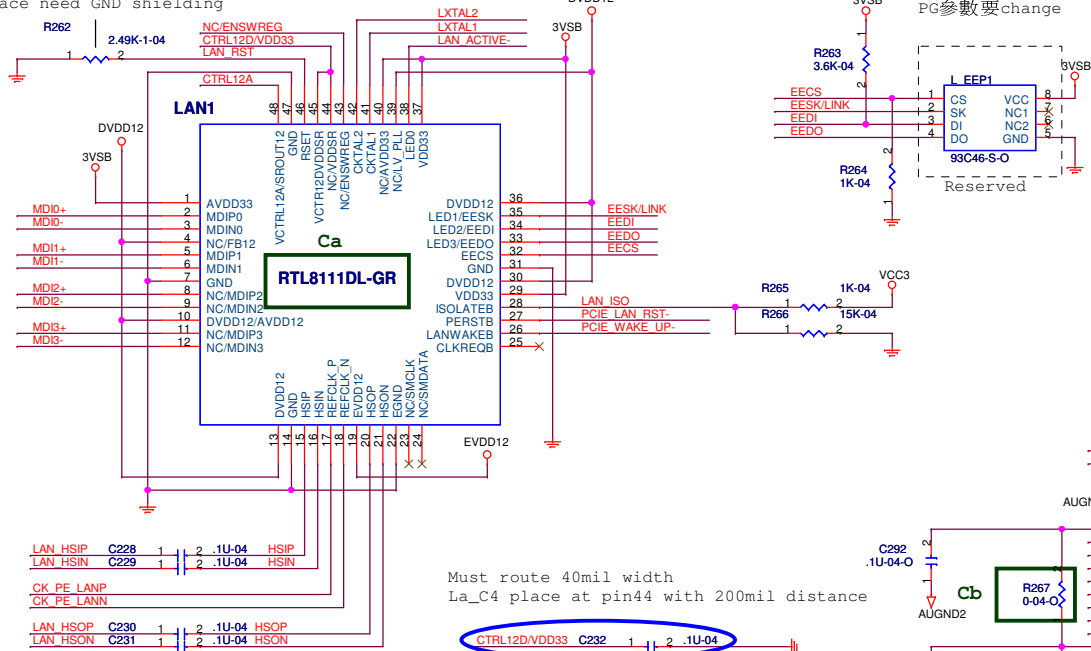
- USBVDDIO to 3VSBD, VCC3, and AUGND2
- LAN HSIP to LAN HSN
- OK PE LANP to OK PE LANN
- LAN HSOP to LAN HSON
- PCIE WAKE UP to PCIE LAN RST
- UV-2 to UV+2
- UV-3 to UV+3

新手提醒:

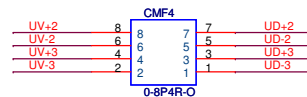
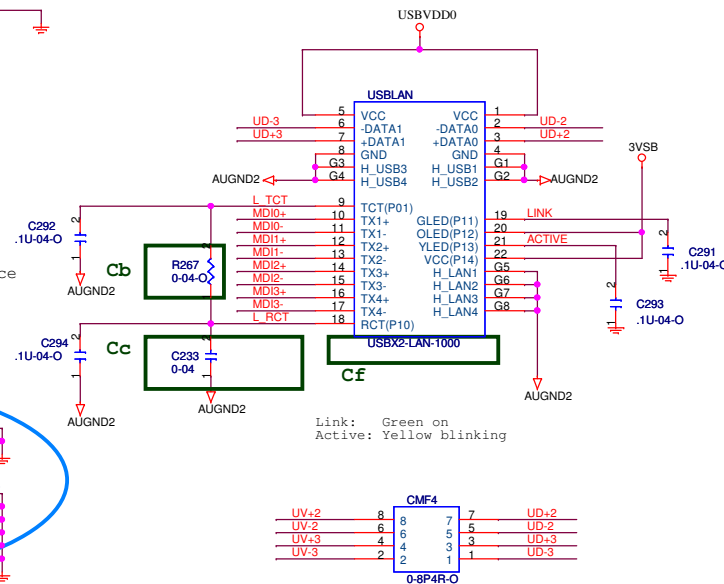
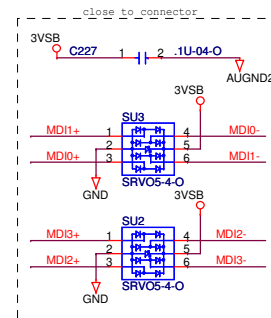
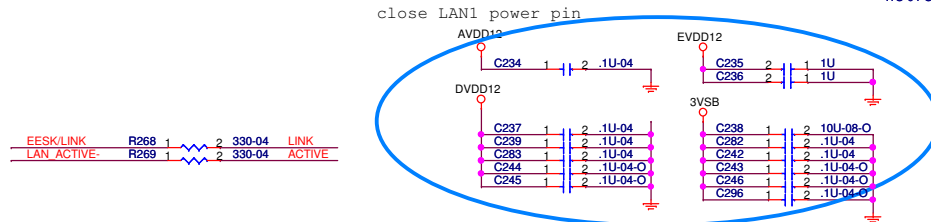
- LAN\_HSOP/N請接到SB的PCIE RX端
- LAN\_HSIP/N請接到SB的PCIE TX端
- LAN\_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

	RTL8111DL-GR 1000M	RTL8102EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8102EL-GR
Cb	X	V
Cc	0-04	.010-04
Cd	X	V
Ce	V	X
Cf	USBX2-LAN-1000	USBX2-LAN-100

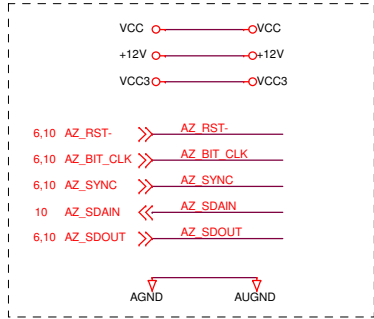
	RTL8111D	RTL8102E
AVDD33 VDD33	<b>3.3V</b> 3VSB供應	<b>3.3V</b> 3VSB供應
CTRL12A	SWitching Output	<b>1.2V</b> pinself 供應
DVDD12	<b>1.2V</b> CTRL12A供應	<b>1.2V</b> pinself 供應
EVDD12	<b>1.2V</b> CTRL12A供應	<b>1.2V</b> pinself 供應



```
Must route 40mil width
La_C4 place at pin44 with 200mil distance
```



## External Connection

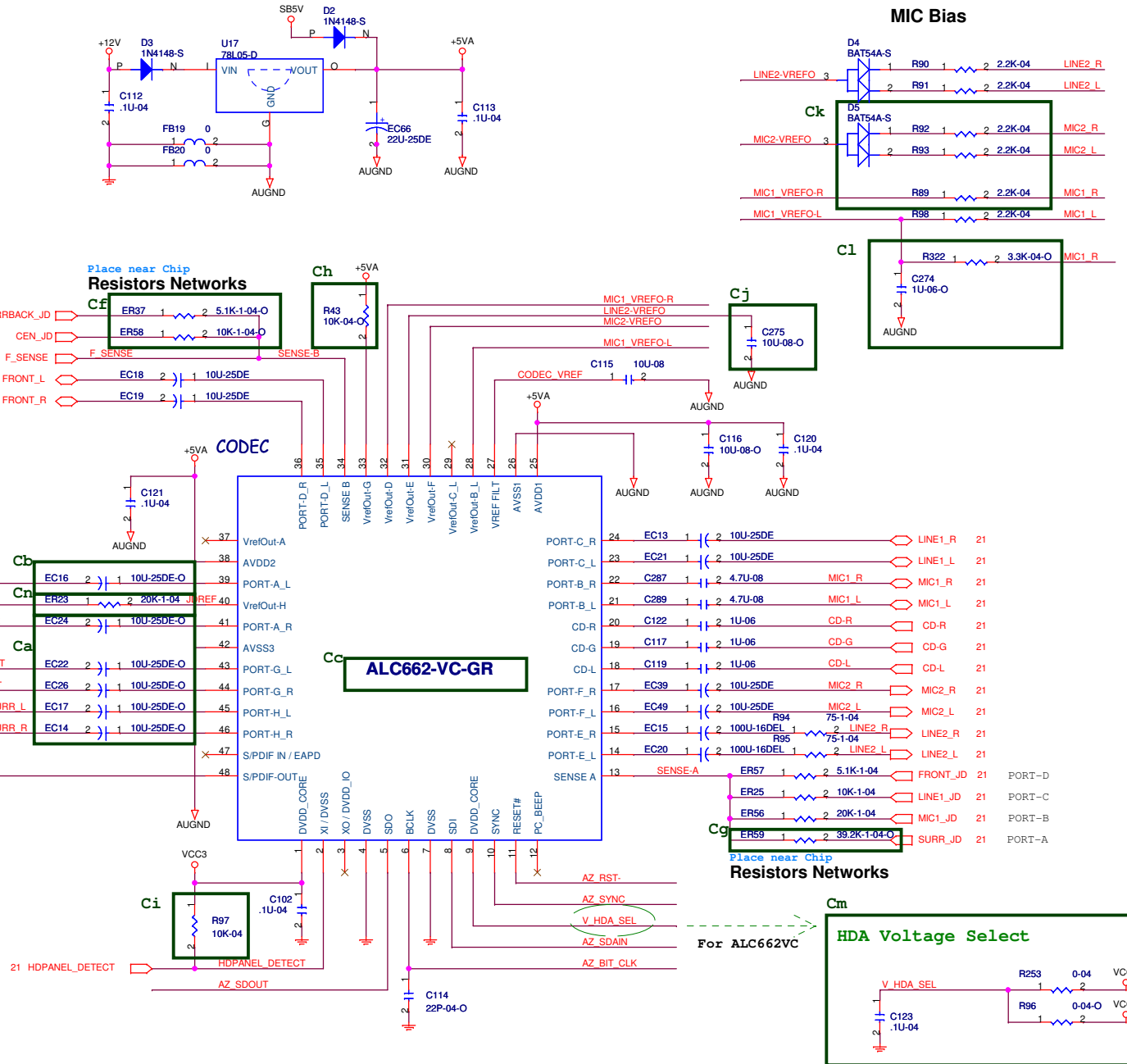


When you found some bug, please inform Ren(ext:665) to update circuit.

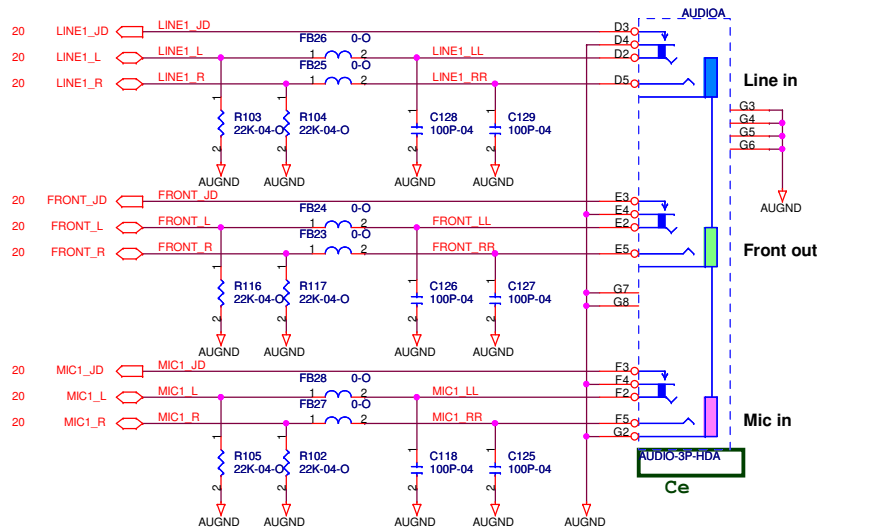
## BOM Difference

Location	ALC888VC 7.1 Ch	ALC662 5.1 CH	VT1708B 7.1CH	VT1708B 5.1CH
Ca	V	X	V	X
Cb	V	X	V	X
Cc	ALC888-GR C2S	ALC662-VC-GRS	VT1708BS	VT1708BS
Cd	V	X	V	X
Ce	AUDIO-6P	AUDIO-3P-HDA	AUDIO-6P	AUDIO-3P-HDA
Cf	V	X	V	X
Cg	V	X	V	X
Ch	V	X	V	X
Ci	V	V	X	X
Cj	X	X	V	V
Ck	V	V	X	X
Cl	X	X	V	V
Cm	VCC1.5/VCC3	VCC1.5/VCC3	VCC3	VCC3
Cn	20K-1-04	20K-1-04	5.1K-1-04	5.1K-1-04

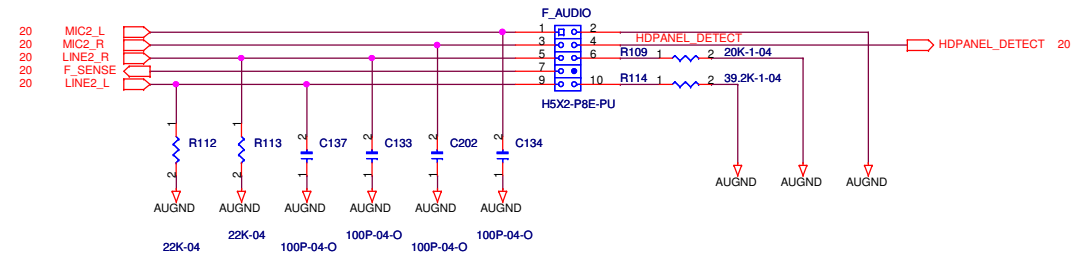
When you change BOM, remember change GPI to inform BIOS use different Verb-Table.



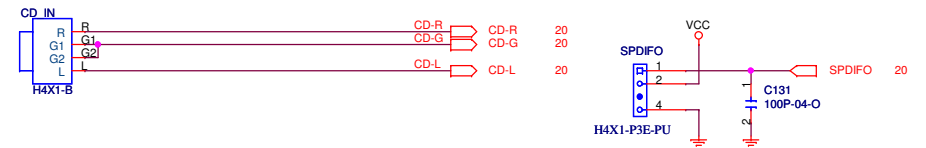
## REAR-AUDIO



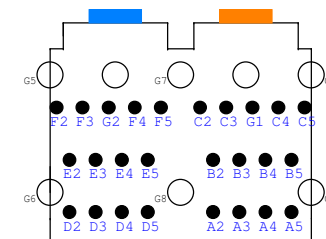
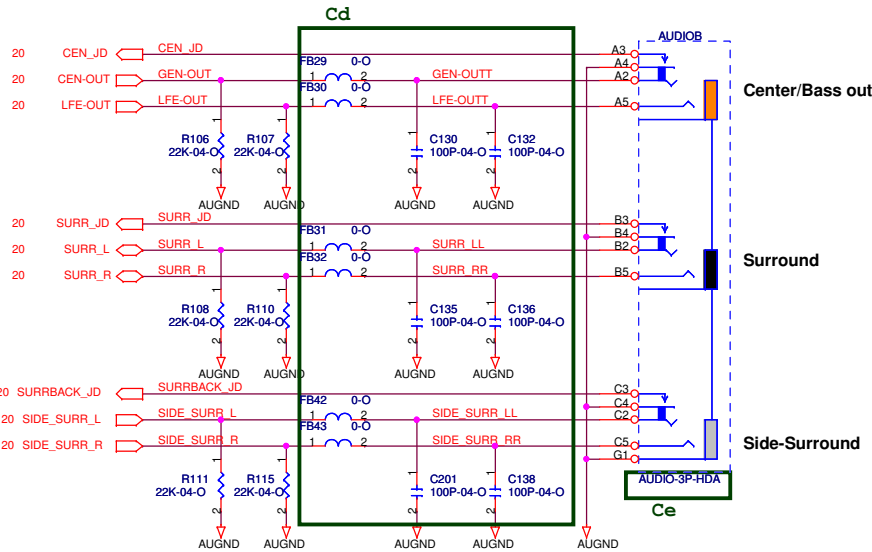
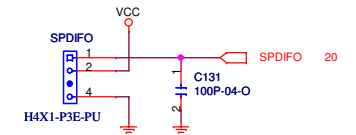
## FRONT-AUDIO



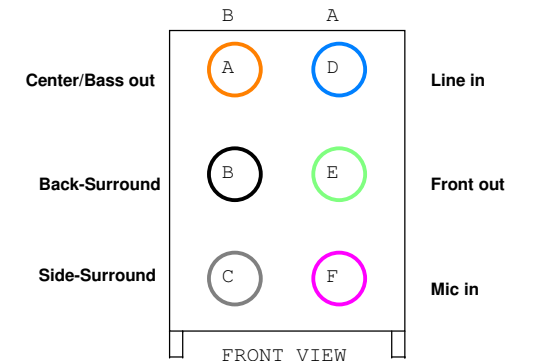
## CD\_IN



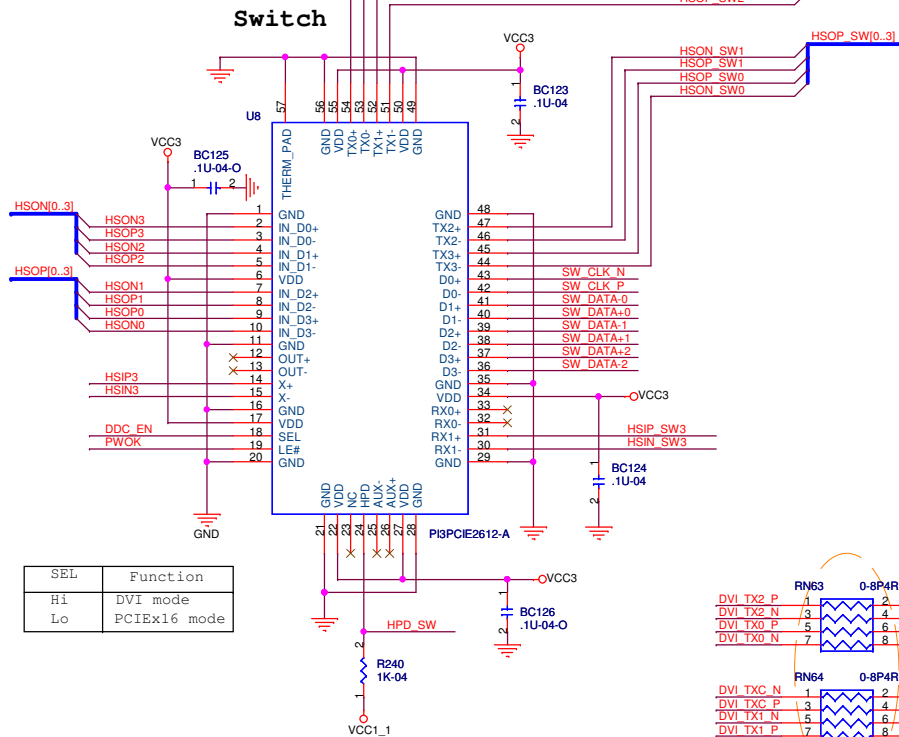
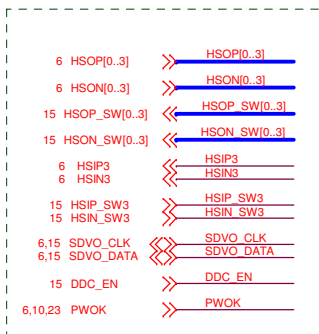
## SPDIF-OUT



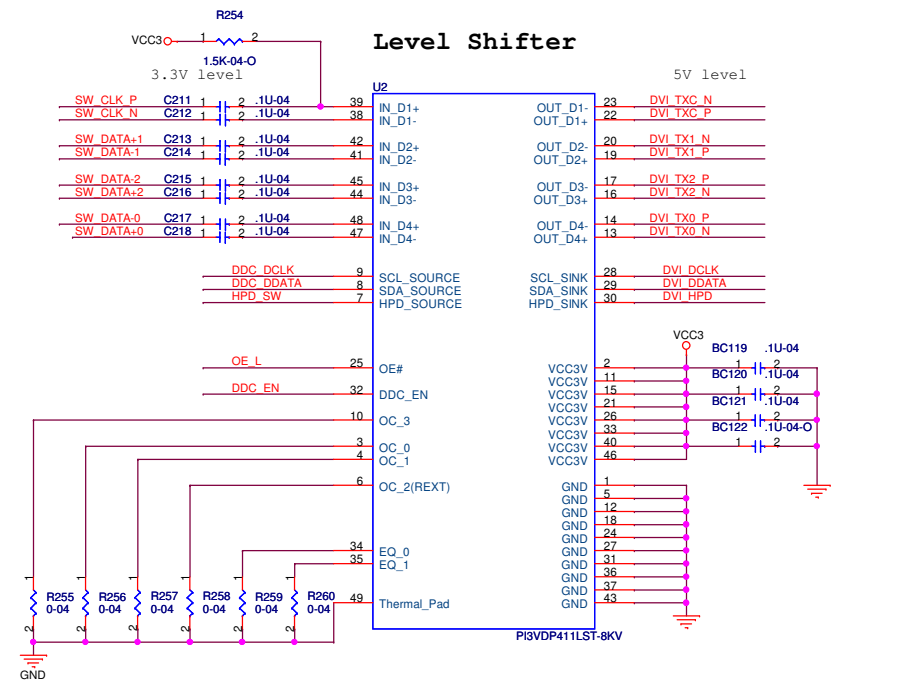
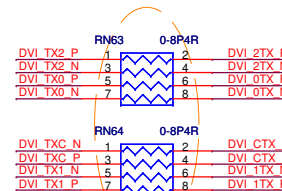
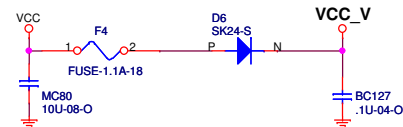
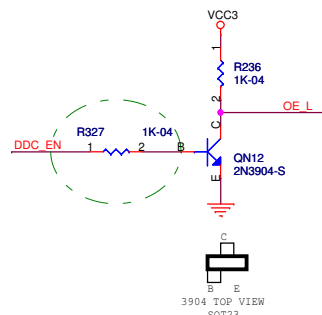
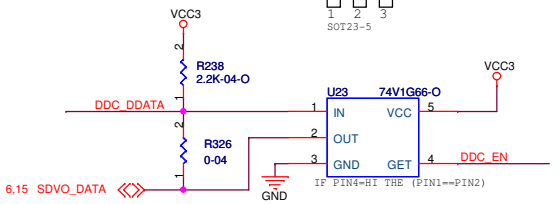
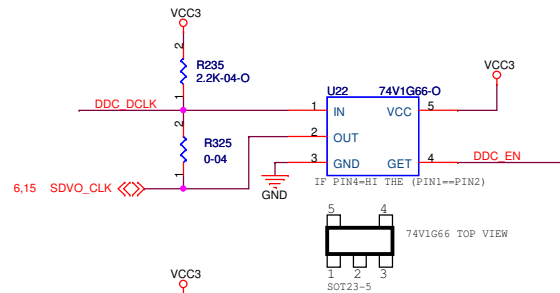
TOP VIEW



FRONT VIEW



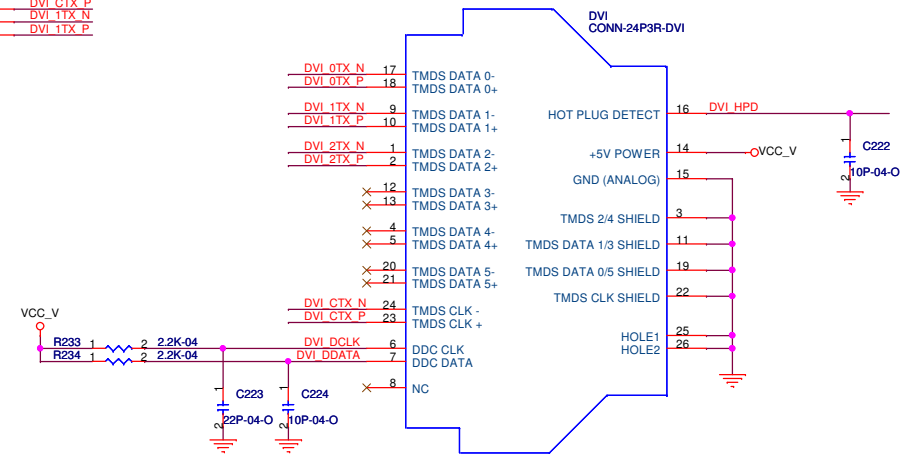
SEL	Function
Hi	DVI mode
Lo	PCIEx16 mode



DDC_EN	Passgate
3.3V	Enable
0	Disable

HD_HPD	Status
Hi	Plugged
Lo	unplugged

HD\_HPD:Internal 100K pull low

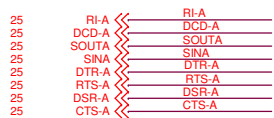


## HW Monitor

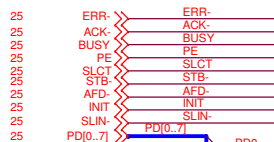


VIN0 for VCORE  
VIN1 for V DIMM  
VIN2 for VCC

## COM



## LPT



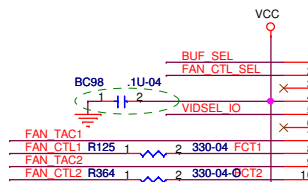
## KB/MS



## IT8713Power On Strapping Options

JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP2	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3	CHIP_SEL		Chip selection in Configuration
JP4	BUF_SEL	1	Output Buffer of PCIRST are open-drain
		0	Output Buffer of PCIRST are push-pull
JP5 : JP7	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 00h
		10	The default value of EC Index 15h/16h/17h is 40h
		01	The default value of EC Index 15h/16h/17h is 20h
		00	The default value of EC Index 15h/16h/17h is 7Fh
JP6	VID_SEL	1	Threshold V of VID is 2.0/0.8 V
		0	Threshold V of VID is 0.8/0.4 V
JP7	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK

DCD-A  
RFA  
CTS-A  
DTR-A  
RTS-A  
DSR-A  
SOUTA  
SINA

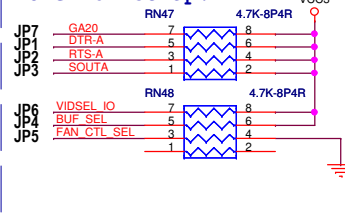


EX\_GPIO\_2  
EX\_GPIO\_1  
EX\_GPIO\_0  
THERM  
GTL\_SEL2  
GTL\_SEL1  
ACPILED  
PWRLED

RSTSW-  
IDE\_RST-  
PWOK  
PCIE\_RST-  
SIOPCIRST-  
LDRO-

SERIRQ  
LFRAME  
LAD0  
LAD1  
LAD2  
LAD3  
SIOKBRST  
GA20  
PCICLK SIO  
SIO CLK

## Power On Strap.



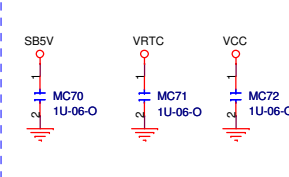
## IT8713F-S/JX-L

BUSY  
 PE  
 SLCT  
 VCC  
 VIN0  
 VIN1  
 VIN2  
 ATXPWRGD/VIN3  
 VIN4  
 VIN5  
 VIN6  
 PCIRSTIN#/VIN7  
 VREF  
 TMPIN1  
 TMPIN2  
 TMPIN3  
 GND4  
 RSMRST#CIRRX/GP55  
 PCIRST4#SCRPPRES#GP10  
 MCLK  
 MDAT  
 KBDAT  
 KBDAT  
 S3\_SW  
 3VSBW#/GP40  
 PWROK2#/GP41  
 SUSAC/GP53  
 PSN#/GP42  
 PANSWH#/GP43  
 GND5  
 PME#/GP54  
 PWONR/GP44  
 SUSB  
 IRRX/GP46  
 VBAT  
 COPEN#  
 VCCB  
 IRTX/GP47  
 DSKCHG#

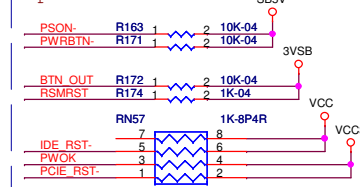
BUSY  
 PE  
 SLCT  
 VCC  
 VIN0  
 VIN1  
 VIN2  
 ATXPWRGD/VIN3  
 VIN4  
 VIN5  
 VIN6  
 PCIRSTIN#/VIN7  
 VREF  
 TMPIN1  
 TMPIN2  
 TMPIN3  
 GND4  
 RSMRST#CIRRX/GP55  
 PCIRST4#SCRPPRES#GP10  
 MCLK  
 MDAT  
 KBDAT  
 KBDAT  
 S3\_SW  
 3VSBW#/GP40  
 PWROK2#/GP41  
 SUSAC/GP53  
 PSN#/GP42  
 PANSWH#/GP43  
 GND5  
 PME#/GP54  
 PWONR/GP44  
 SUSB  
 IRRX/GP46  
 VBAT  
 COPEN#  
 VCCB  
 IRTX/GP47  
 DSKCHG#

SERIRQ  
 LFRAME  
 LAD0  
 LAD1  
 LAD2  
 LAD3  
 SIOKBRST  
 GA20  
 PCICLK SIO  
 SIO CLK

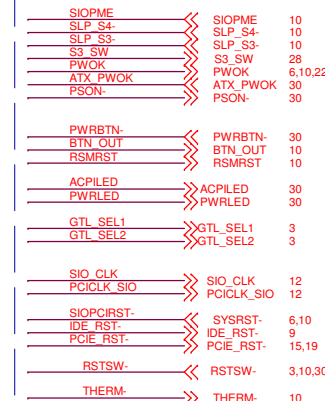
## Place Near To SIO Power Pin



## Open Drain



## ACPI & Others



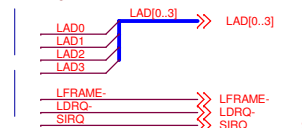
## PECI



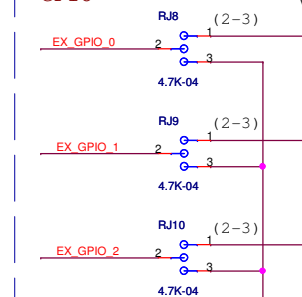
## SMART FAN



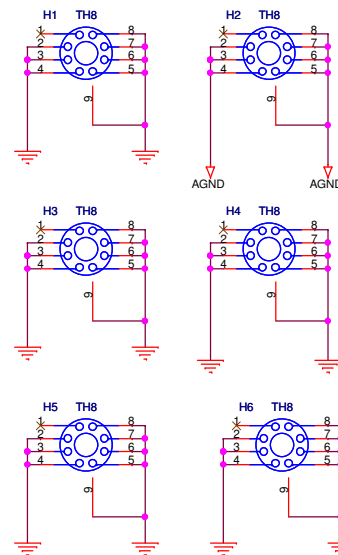
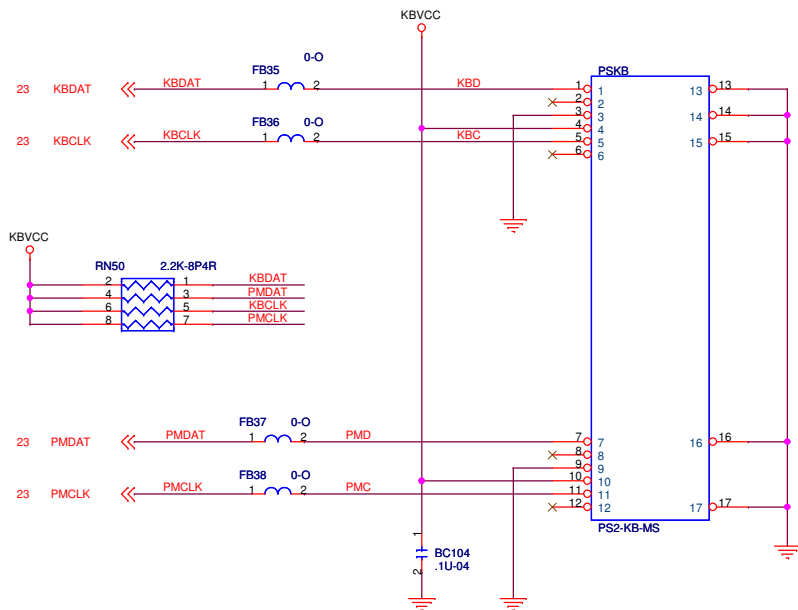
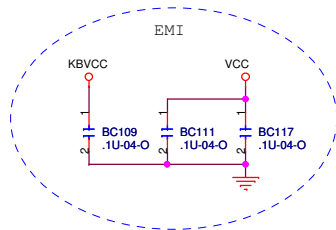
## LPC



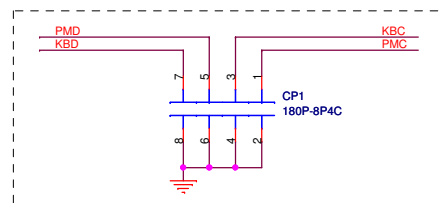
## GPIO

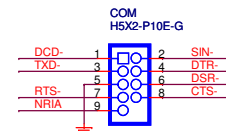
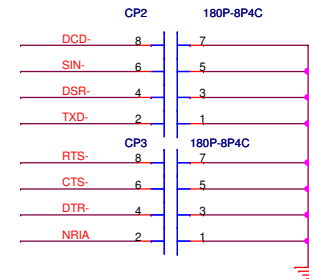
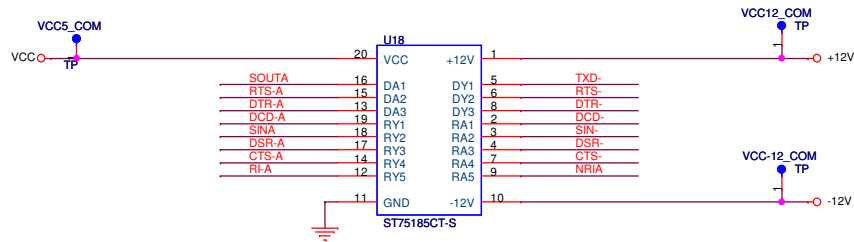
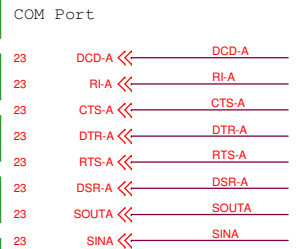


EX\_GPIO\_0 = 0 -> LPT HW Enable  
EX\_GPIO\_0 = 1 -> LPT HW Disable



PLACE NEAR CONNECTOR

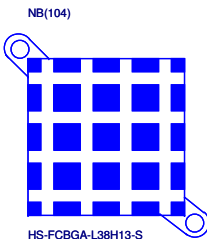




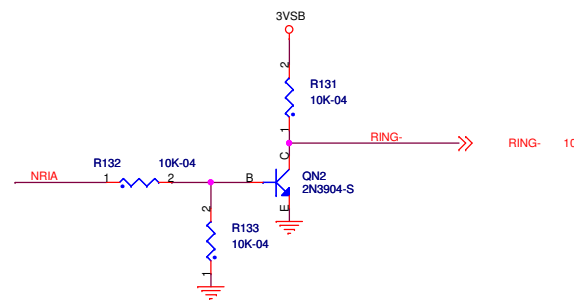
For 104



For 103



If need 25mm height :  
20-120-010937 or 20-120-011420



### PCB Impedance control

Impedance (ohm)	Trace Width (mil)	Trace Length (S/W/S)	Pre-preg
60	5	(20/5/20)	2116
50	4	(50/4/50)	1080
42	6	(50/6/50)	1080

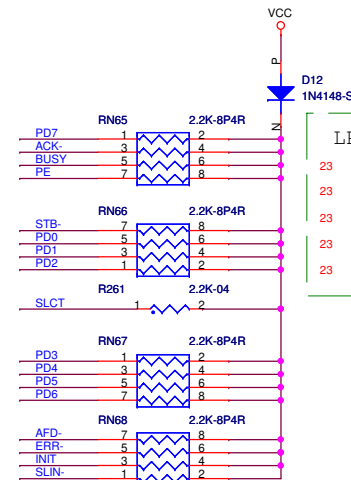
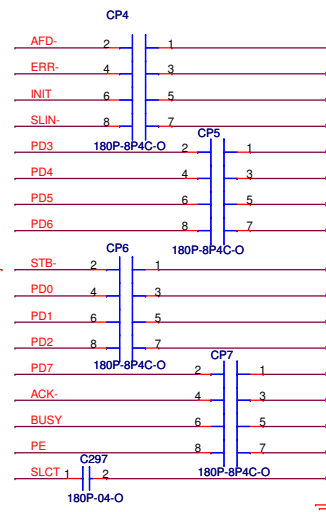
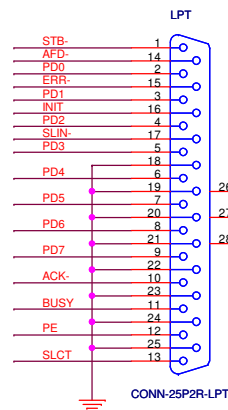
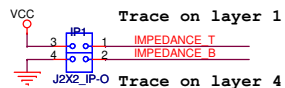
### 1)Circuit type 1

Layer 1:TOP

Layer 2:PWR

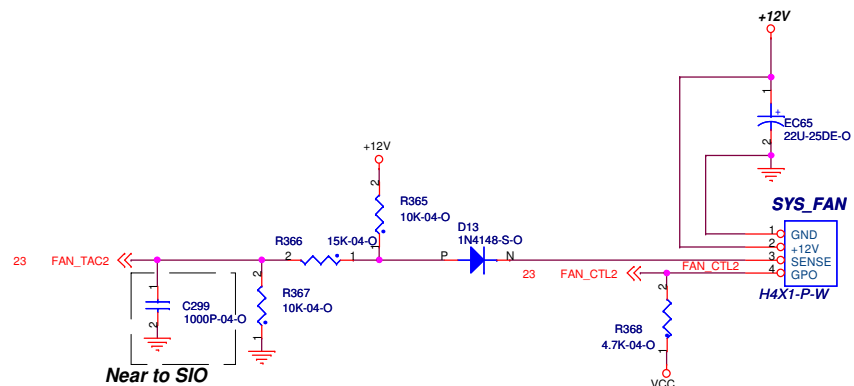
Layer 3:GND

Layer 4:BOTTOM



### LPT





## Temperature Monitor

23 SIO\_VREF << SIO\_VREF

3.23 HM\_AGND << HM\_AGND

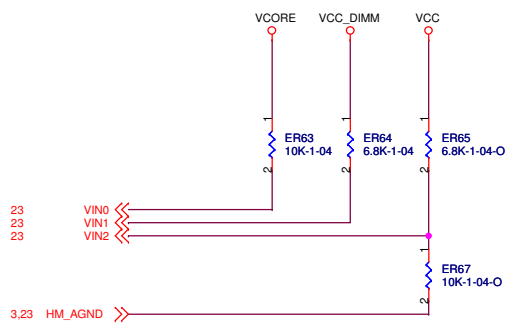
3.23 TMP\_CPU << TMP\_CPU

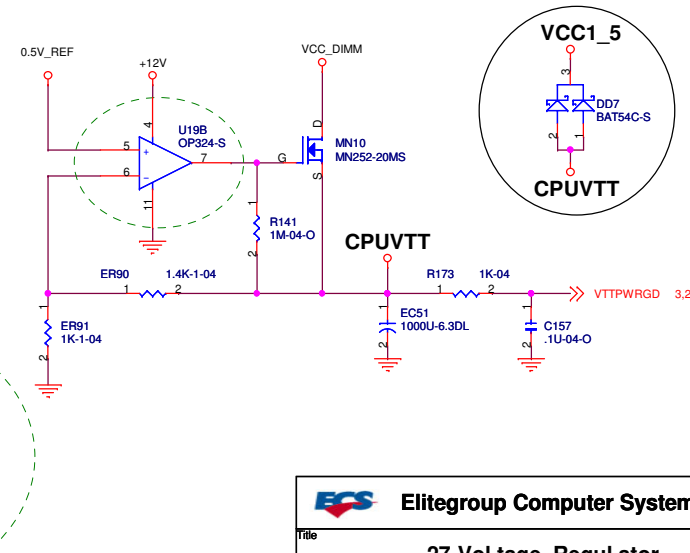
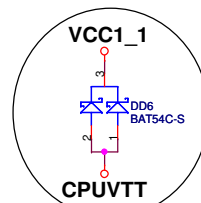
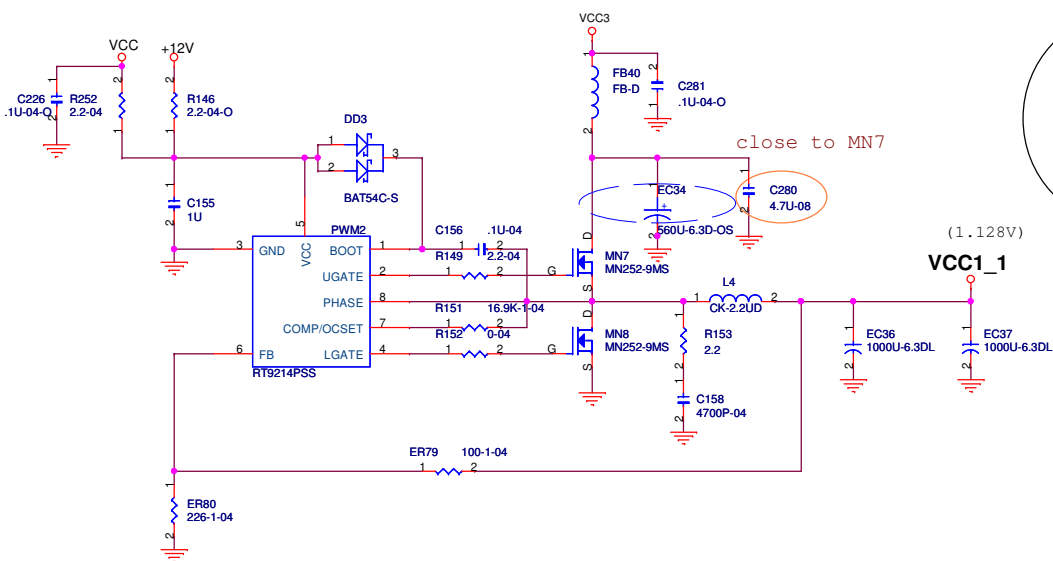
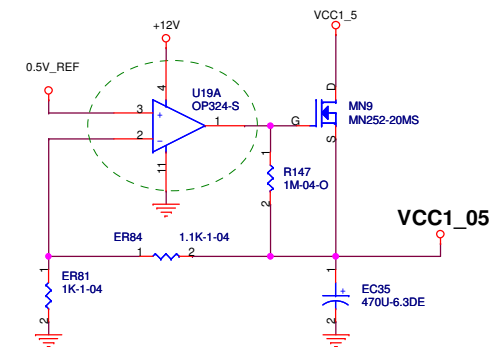
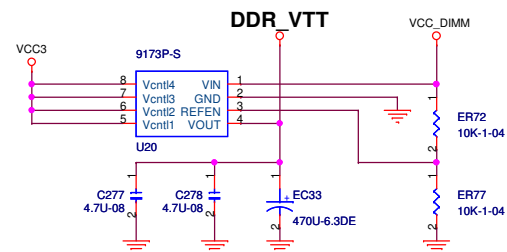
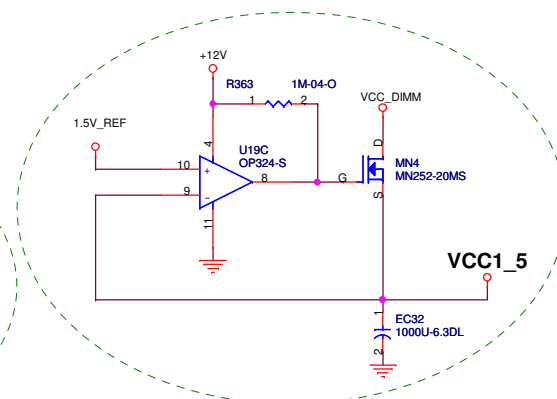
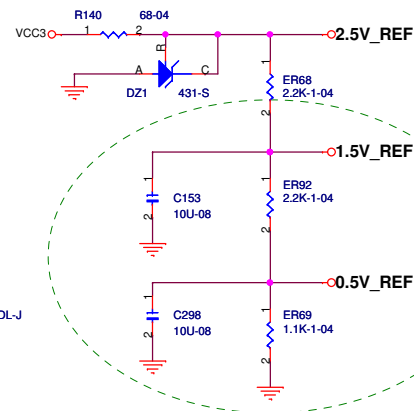
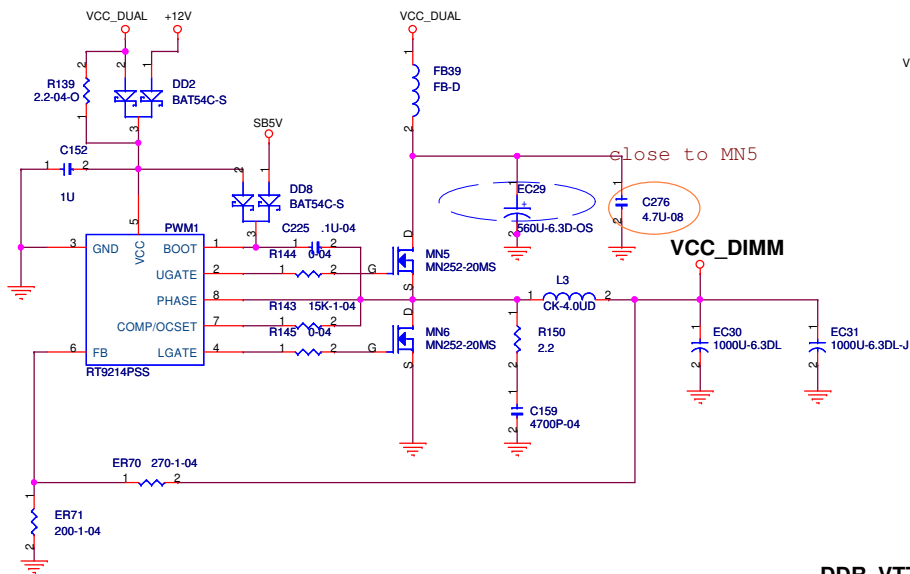
C8 1U-06

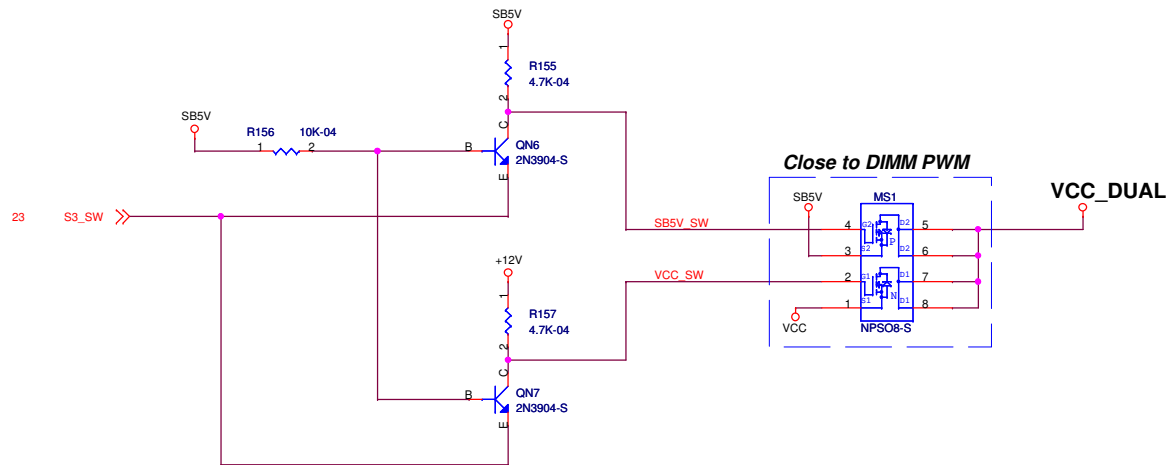
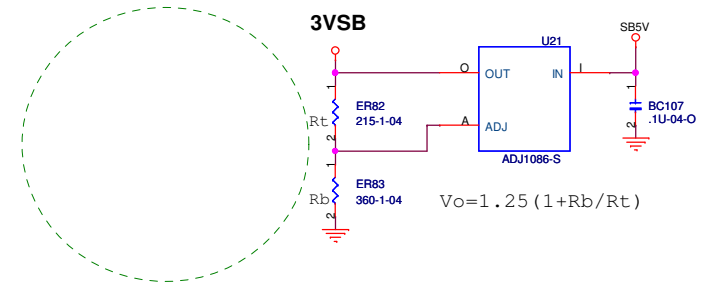
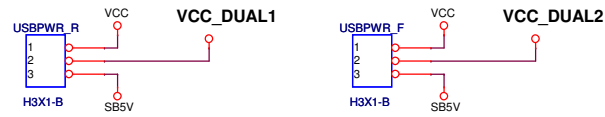
C9 2200P-04

CPU\_THERMDC << CPU\_THERMDC 3.23

CPU\_THERMDA << CPU\_THERMDA 3.23







**Memory Power Output Control**

	<i>VCC_DUAL</i>	<i>ATX_PWOK</i>	<i>SLP_S4-</i>	<i>SLP_S3-</i>	<i>S3_SW</i>
<i>S0</i>	<i>VCC</i>	<i>1</i>	<i>1</i>	<i>1</i>	<i>1</i>
<i>S1</i>	<i>VCC</i>	<i>1</i>	<i>1</i>	<i>1</i>	<i>1</i>
<i>S3</i>	<i>SB5V</i>	<i>0</i>	<i>1</i>	<i>0</i>	<i>0</i>
<i>S4</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>1</i>
<i>S5</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>1</i>



